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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/527,422	03/17/2000	Alexander I. Krymski	08305-070001	4176

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EXAMINER	
MISLEH, JUSTIN P	

ART UNIT	PAPER NUMBER
2622	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/527,422	KRYMSKI ET AL.	
	Examiner	Art Unit	
	Justin P. Misleh	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2006 and 31 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 6 and 8 - 40* is/are pending in the application.

4a) Of the above claim(s) *3, 11 - 15, 17, and 22 - 40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,16 and 18* is/are rejected.

7)☒ Claim(s) *6, 8 - 10 and 19 - 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on January 5, 2006 and January 31, 2006, with respect to the rejection of claims 1 – 6, 9 – 11, 16 –1 9, and 21 – 22 under 35 U.S.C. §102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Merrill et al.

2. Furthermore, since this Office Action present a new ground of rejection on original claims, this Office Action is Non-Final.

Election/Restrictions

3. In the Response, filed December 29, 2003, Applicant elected the species directed to Figure 8 and with Claims 1 – 6, 8 – 10, 16 – 19, 21, 22, 29, 32, 38 and 39 are readable on the elected species. In the Office Action, mailed September 10, 2004, the Examiner selected Claims 1 – 6, 8 – 11 and 16 – 22 as being closely related to the elected species. However, after careful consideration, Claims 3, 11, 17, and 22 are hereby withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Specifically, Claims 3 and 17 are directed towards the A/D converting features of nonelected figure 4 as described on page 7 (lines 13 – 21) of the specification, and Claims 11 and 22 are directed towards the buffer circuit with p-MOS source follower features of nonelected figure 2.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1, 2, 4, 5, 16, and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill et al. (US 6 512 544 B1).

6. For **Claim 1**, Merrill et al. disclose, as shown in figures 5, 7, 9, and 10 and as stated in column 6 (lines 1 – 67), column 7 (lines 52 – 67), and column 8 (lines 1 – 9 and 30 – 37), a method of processing pixel levels, the method comprising:

clamping a pixel readout line ("column line" – see figure 5) to a voltage level less than a voltage corresponding to a pixel signal (see column 6, lines 51 – 56, column 7, lines 61 – 67, and column 8, lines 1 – 6);

subsequently coupling (coupling via the rows select transistor 110) the pixel readout line ("column line") to an output of an n-MOS source-follower (source-follower amplifier 100) and reading out the pixel signal onto the pixel readout line ("column line") through n-MOS source-follower (Merrill et al. expressly state that the "COLRESET signal is asserted prior to the assertion of each ROWSEL signal"; see "integration" and "COLRESET" periods in figure 7 and also see column 8, lines 1 – 3. Furthermore, Figures 9 and 10 and column 10, lines 3 – 27, indicate a positive voltage representing the pixel signal output onto the "column line". Finally, Merrill et al. expressly state "the column line 108 may be reset to ground potential by a column-reset switch 114"; see column 6, lines 51 – 56).

While Merrill et al. disclose clamping a column bus and subsequently outputting a pixel signal to the column bus, Merrill et al. do not disclose storing a signal corresponding to the pixel signal that was read out.

However, **Official Notice** (MPEP § 2144.03) is taken that both the concepts and advantages of storing a signal corresponding to a pixel signal that was read out are well known and expected in the art. At the time the invention was made, it would have been obvious to one with ordinary skill in the art to store a signal corresponding to a pixel signal that was read out for the advantage having the signal available for processing at a later time.

7. As for **Claim 2**, Merrill et al. disclose, as shown in figure 5 and 7 and as stated in column 6 (lines 51 – 56), wherein clamping the pixel readout line ("column line") includes discharging a capacitance (no bus capacitor or phantom bus capacitor is actually shown in figure 5; however, a bus capacitance naturally exists on the "column line" and would be discharged upon activating transistor 114) on the pixel readout line.

8. As for **Claim 4**, Merrill et al. disclose, as shown in figure 7 and as stated in column 7 (line 61) – column 8 (line 3), wherein discharging the pixel readout line ("column line") includes disabling a pixel selection switch (row select transistor 110).

As clearly shown in figure 7, the pixel (80) is completely cutoff from the column line (108) during discharging the of the column line (when "COLRESET" is asserted).

9. As for **Claim 5**, Merrill et al. disclose, as shown in figures 5 and 7 and as stated in column 7 (line 61) – column (line 3), wherein discharging the pixel readout line ("column line") includes enabling a switch to couple the pixel readout line to ground (114 – see figure 5).

10. For **Claim 16**, Merrill et al. disclose, as shown in figures 5, 7, 9, and 10 and as stated in column 6 (lines 1 – 67), column 7 (lines 52 – 67), and column 8 (lines 1 – 9 and 30 – 37), an imager comprising:

a pixel readout line ("column line" – see figure 5);

an active pixel sensor (see figure 5) including an n-MOS source-follower (source-follower amplifier 100) through which signals sensed by the sensor can be read out to the pixel readout line ("column line"), a first switch (row select transistor 110) that can be enabled to read out signals from the sensor, and a reset switch (reset transistor 88);

a controller (not explicitly shown; however, necessary for operation) configured to provide control signals to cause the pixel readout line ("column line") to be clamped to a voltage level less than a voltage corresponding to a pixel signal (see column 6, lines 51 – 56, column 7, lines 61 – 67, and column 8, lines 1 – 6), and subsequently to cause the sensor signal to be read out (coupling via the rows select transistor 110) through the n-MOS source-follower to the pixel readout line (Merrill et al. expressly state that the "COLRESET signal is asserted prior to the assertion of each ROWSEL signal"; see "integration" and "COLRESET" periods in figure 7 and also see column 8, lines 1 – 3. Furthermore, Figures 9 and 10 and column 10, lines 3 – 27, indicate a positive voltage representing the pixel signal output onto the "column line". Finally, Merrill et al. expressly state "the column line 108 may be reset to ground potential by a column-reset switch 114"; see column 6, lines 51 – 56).

While Merrill et al. disclose an active pixel sensor and a controller for clamping a column bus and subsequently outputting a pixel signal to the column bus, Merrill et al. do not disclose a

signal processing circuit that can be coupled to the pixel readout line and storing a signal corresponding to the pixel signal that was read out in the processing circuit.

However, **Official Notice** (MPEP § 2144.03) is taken that both the concepts and advantages of including a signal processing circuit that can be coupled to the pixel readout line and storing a signal corresponding to the pixel signal that was read out in the processing circuit are well known and expected in the art. At the time the invention was made, it would have been obvious to one with ordinary skill in the art to include a signal processing circuit that can be coupled to the pixel readout line and storing a signal corresponding to the pixel signal that was read out in the processing circuit for the advantage of increasing the processing to increasing the signal-to-noise ratio of the signal at a later time.

11. As for **Claim 18**, Merrill et al. disclose, as shown in figure 5, including a third switch (114) coupled between the pixel readout line ("column line") and ground (see figure 5), wherein the controller is configured to pride a control signal (116) to cause the pixel readout line ("column line") to be clamped by enabling the third switch (see figure 7).

Allowable Subject Matter

12. **Claims 6, 8 – 10 and 19 – 21** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

For **Claims 6 and 19**, while the closest prior art at least discloses an active pixel sensor and a controller for clamping a column bus and subsequently outputting a pixel signal to the column bus and a processing circuit for storing the signal;

the closest prior does not teach or fairly suggest an imager with a processing circuit wherein the processing further includes (or correspondingly performs) a capacitive storage node to be clamped to a voltage less than a voltage corresponding to a sensor signal on appearing on a pixel readout line (as a pixel sensor output), and subsequently causing the pixel readout line to be coupled to the capacitive storage node.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 571.272.7313. The Examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, David L Ometz can be reached on 571.272.7593. The fax phone number for the organization where this application or proceeding is assigned is 571.273.3000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
March 18, 2006

DAVID OMETZ
SUPERVISORY PATENT EXAMINER